



# **i403 PC-CARD**

# **USER'S GUIDE**

### REVISION HISTORY

ISSUE	PAGES	AUTHOR	NOTES
A	16	PS	FIRST ISSUE
B	16	PS	Corrected 60Way IDC Pinout Table
1	24	PS	S/W SECTION
2	17	BP	REMOVED SOFTWARE SECTION TO PCCARDGO.DOC
3	17	PS	ERROR WITH LOGIC IN DESCR. OF IRQAUTOCLR (now active low)

# CONTENTS

<b>1.0 OVERVIEW</b> .....	<b>4</b>
<b>2.0 PROGRAMMING INTERFACE</b> .....	<b>5</b>
<b>IO<sub>n..(n+7)</sub> DATA/STATE REGISTERS (IDX 0,1,2,3,4)</b> .....	<b>7</b>
<b>IO BANK DIRECTIONS (IDX 5)</b> .....	<b>7</b>
<b>AUX SETUP REGISTER (IDX 6)</b> .....	<b>8</b>
<b>REVISION/MISC STATUS REGISTER (IDX 6)</b> .....	<b>8</b>
<b>SETUP REGISTER (IDX 7)</b> .....	<b>9</b>
<b>BANK<sub>n</sub> DIR CTRL REGISTERS (IDX 8,9,A,B,C)</b> .....	<b>11</b>
<b>TIMER 0,1&amp;2 REGISTERS (IDX 10h,11h,12h)</b> .....	<b>12</b>
<b>TIMER CTRL REGISTER (IDX 13h)</b> .....	<b>12</b>
<b>3.0 HARDWARE SPECIFICATION</b> .....	<b>13</b>
DIGITAL I/O: .....	13
TIMERS .....	13
MISCELLANEOUS.....	14
PINOUTS .....	14
IDC BREAKOUT BOARD OPTION:.....	15
<b>4. SOFTWARE</b> .....	<b>17</b>
<b>4.1 UNIVERSAL DRIVER</b> .....	<b>17</b>
<b>4.2 C SOURCE CODE</b> .....	<b>17</b>
<b>5.0 OPERATIONAL PRECAUTIONS</b> .....	<b>18</b>

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## 1.0 OVERVIEW

The I403 card is a general purpose Digital PIO card with the following features:

- 40 BI-DIRECTIONAL DIGITAL I/O LINES
- ANY I/O CAN BE PROGRAMMED AS AN INPUT OR AN OUTPUT
- ANY I/O CAN BE SET AS AN OPEN DRAIN TYPE DRIVER
- 47K PULL RESISTOR ON EVERY I/O TO A SWITCHABLE 0V OR 5V VOLTAGE SOURCE. POWER ON STATE IS PULL DOWN SO ALL I/Os DEFAULT TO LOW-HIZ.
- 3-CHANNEL COUNTER TIMER WITH ON CARD 4MHz OSCILLATOR. HARDWARE TIMING PERIODS FROM 250ns TO 6.5s POSSIBLE (LONGER IF TIMER IS RETRIGGERED BY SOFTWARE)
- 4MHz MASTER OSCILLATOR ON CARD
- TIMER 0 CAN BE USED TO GENERATE INTERRUPTS
- "SNAP-SHOT" MODE ALLOWS TIMER 0 TO SAMPLE INPUTS & INTERRUPT PC GIVING ACCURATE AND PREDICTABLE SAMPLE PERIOD (AVOIDING INTERRUPT LATENCY)
- TIMERS 1 & 2 ARE "UN-COMMITTED" AND CAN BE USER DRIVEN. TIMER 2 CAN ALSO BE CONFIGURED TO BE USER-DRIVEN.
- FREQUENCY COUNTER MODE, ALLOWS DIRECT FREQUENCY MEASUREMENT OF TTL SIGNALS FROM 1Hz TO 8MHz (ACCURACY TYP 0.5% FROM 40Hz TO 8MHz)
- INTERNAL CLOCK DIVIDER GENERATES 1MHz, 100KHz & 10KHz FOR TIMER AND EXTERNAL USE. THIS CLOCK CAN BE TRI-STATED SO THAT IT CAN BE OVER-DRIVEN IF REQUIRED.
- "SLEEP" MODE DISABLES CLOCK REDUCING POWER CONSUMPTION
- LOW POWER CONSUMPTION FOR PORTABLE APPLICATIONS
- TYPE II CARD IS PCMCIA 2.0 COMPLIANT
- FLEXIBLE CIRCUIT TERMINATES ALL I/O LINES IN A HIGH DENSITY IDC CONNECTOR OR TRIGGER TERMINAL BLOCKS FOR SIMPLE INTERFACING.

## 2.0 PROGRAMMING INTERFACE

The I403 decodes the incoming PCMCIA interface. It maps the CIS EPROM to 0-3FF,800-BFF etc. in attribute space. The range 400-7FF is occupied by the PCMCIA config register inside the FPGA (it repeats every byte). Both the CIS and config register are always active.

The config register is used as a master enable, as defined by PCMCIA 2.01. That is, when a valid config is written in bits0..5 the card's I/O interface may function. Until this has happened, the card's I/O interface is disabled.

A config value of 1 will enable interrupts (if generated and secondary enabling is ON) whereas a value of 2 will disable interrupts. Bit6 of the register controls level or pulse mode nIRQ operation and bit7 acts as a soft reset when set (the reset does not clear bit7 but a subsequent write to the config register to return bit 7 to zero should not attempt to load data into bits 6..0 of the register as they will still clear. This should be done as a separate operation.)

BIT0	Config value LSB
BIT1	.
BIT2	.
BIT3	.
BIT4	.
BIT5	Config value MSB
BIT6	Level mode nIRQ if set
BIT7	apply internal RESET when set

### CONFIG Register at 400h in Attribute

All I403 functions are accessed via two I/O ports (as mapped by the host controller). The I403 only decodes A0, giving an Index register and a Data register (IR,DR). The IR is at the even address. It is 8-bits wide and is read/write. The IR selects which internal register is to be read/written via the DR (cf 82365 PCIC). The DR is also 8-bits wide. The I403 hence only uses nCE1 from the

PCMCIA interface. It is the job of the host socket controller to map the IR and DR registers into the system's IO space.

The following list shows the indexes of the various registers in the I403 FPGA:

IR	DR write	DR read	
0	IO1..8 DATA	IO1..8 i/p STATE	BANK0
1	IO9..16 DATA	IO9..16 i/p STATE	BANK1
2	IO17..24 DATA	IO17..24 i/p STATE	BANK2
3	IO25..32 DATA	IO25..32 i/p STATE	BANK3
4	IO33..40 DATA	IO33..40 i/p STATE	BANK4
5	NOT USED	IO BANK DIRECTIONS	
6	AUX SETUP REG	REVISION/MISC STATUS	
7	SETUP REG	SETUP REG	
8	BANK0 DIR CTRL	NOT USED	
9	BANK1 DIR CTRL	NOT USED	
Ah	BANK2 DIR CTRL	NOT USED	
Bh	BANK3 DIR CTRL	NOT USED	
Ch	BANK4 DIR CTRL	NOT USED	
Dh	NOT USED	NOT USED	
Eh	NOT USED	NOT USED	
Fh	NOT USED	NOT USED	
10h	TIMER 0	TIMER 0	
11h	TIMER 1	TIMER 1	
12h	TIMER 2	TIMER 2	
13h	TIMER CTRL	TIMER CTRL	

### Index Allocations in the I403

The detailed operation of each register will now follow:

## ***IO<sub>n..(n+7)</sub> DATA/STATE REGISTERS (IDX 0,1,2,3,4)***

If an IO pin is set as an output via the DIR CTRL register, then the DATA bit sent to that pin will directly control its output state. The 40 IO pins are grouped as 5 banks of 8 pins. All banks are identical EXCEPT bank 0 which has extra features. The byte sent to the DATA register for a bank corresponds bit-for-bit with the IO pins with the LSBit of the byte controlling the lowest numbered IO pin.

Reading the STATE register will return the bit-mapped state of the bank's IO pin input latches (transparent OR frozen depending on the mode of operation).

The power on state of all IO DATA registers is 00h.

## ***IO BANK DIRECTIONS (IDX 5)***

This is an 8-bit read only register. With all but the exception of BANK0, a BANK's set of 8 IO pins can only be set up as all inputs or all outputs. BANK0 has finer resolution to allow any number of inputs and outputs within the 40 total IO pins. The structure of the register is as follows:

BIT0	DIRECTION OF BANK0 PIN1
BIT1	DIRECTION OF BANK1
BIT2	DIRECTION OF BANK2
BIT3	DIRECTION OF BANK3
BIT4	DIRECTION OF BANK4
BIT5	DIRECTION OF BANK0 PIN2
BIT6	DIRECTION OF BANK0 PINS3&4
BIT7	DIRECTION OF BANK0 PINS5,6,7&8.

A '1' in any bit position means that the IO pin is an output.

## **AUX SETUP REGISTER (IDX 6)**

This register is write only and provides a "grab-bag" of left over control bits. Its layout is as follows:

BIT0	IOPULLUP DIRECTION 0=pull down 1=pull up (POS=0) (all IO pins have 47K connected to a buffered version of this signal).
BIT1	1=ENABLE DIRECT CONTROL OF GATE0 (POS=0)
BIT2	CONTROL BIT FOR GATE0 (POS=0)
BIT3	ENABLE IOPIN 1 TO BE /(OUT0) (IF THE PIN IS SET AS AN OUTPUT) (POS=0) ("/" means inverse)
BIT4	MUST BE '0' (POS=0)
BIT5..7	RESERVED (KEEP AT '0')

NB: POS="POWER ON STATE" (and after a reset)

## **REVISION/MISC STATUS REGISTER (IDX 6)**

The bottom 6 bits give the chip ID and revision code. The top two bits are used for status monitoring, as follows:

BIT0	ID CODE LSBit
BIT1	.
BIT2	ID CODE MSBit
BIT3	REV CODE LSBit
BIT4	.
BIT5	REV CODE MSBit
BIT6	nIRQSTATE
BIT7	OUT0STATE

The ID code will be 4 (for I403). The REV code will follow the revision of the GATE ARRAY and is currently at 3.

nIRQSTATE reflects the status of the internal +ET flip flop used to turn pulsed IRQs into level IRQs. It can be set via the SETUP REG and is cleared by the rising edge of a correctly routed interrupt.

OUT0STATE is the current state of the OUT0 pin of COUNTER TIMER 0.

## **SETUP REGISTER (IDX 7)**

This register controls the major housekeeping functions of the FPGA. Its layout is as follows (NB POS="Power On State"):

BIT0 CLK DIVISOR LSBit POS=0

BIT1 CLK DIVISOR MSBit POS=0

The following clock frequencies can be obtained:

DIVISOR=0: CLKOUT from FPGA goes hi-z allowing it to be over-driven from the user interface; DIVISOR=1

CLKOUT=1MHz, DC=50%; DIVISOR=2

CLKOUT=100KHz, DC=90%; DIVISOR=3

CLKOUT=10KHz, DC=90%. Duty Cycle (DC) measured as  $100 \times \text{Thigh} / \text{CLKOUTPERIOD}$ . Note that CLKOUT is connected to the on-card COUNTER TIMER pin CTCLK0.

BIT2 IRQEN POS=0. Master interrupt enable. Only active if config value is 1. IRQs enabled if BIT 2 is set.

BIT3 IRQSOURCE POS=0. Selects the IRQ source, between OUT0 from counter timer 0, or from nUIRQ from the user interface. The interrupt is active at the rising edge. BIT3=1 selects nUIRQ.

BIT4 LATCHMODEEN POS=0. When BIT 4 is high, OUT0 will latch BANK input pin states into internal transparent latches on transition from a 0 to a 1. This is "snapshot" mode. The OUT0 low going strobe pulse can be set with CTmode 1 or 2 (for example). When BIT4 is low, the latches operate in transparent mode.

BIT5 nIRQCOMPLETE POS=0. This bit connects directly to the interrupt detect flip flop's nPRESET input. Leaving it low when level mode interrupts are selected will prevent interrupts and cause the nIRQSTATE status to read back as '1'. Setting it high will release the preset state. A rising edge from an interrupt will cause the f/f to reset. Use this bit, set high-low-high to clear the interrupt f/f for level mode operation. This bit has no effect for pulse mode interrupts.

- BIT6**      `nIRQAUTOCLR POS=0`. When clear, and Level mode interrupts are selected, this feature offers a more efficient IRQ complete mechanism than BIT5. Any read from `DR=0..4` (i.e. the IO PIN STATUS registers) will clear the interrupt f/f. This is useful for "snapshot" mode, when `OUT0` pulses low cyclically and `LATCHMODEEN` is true. Then, with level mode interrupts, and the IRQ source set to `OUT0`, an interrupt will be generated each time new IOPIN STATUS data is available. Reading this data, will automatically clear the IRQ. BIT5 is "dontcare" if BIT6 is clear.
- BIT7**      `nSLEEP POS=0`. When this bit is '0', the master 4MHz oscillator is disabled, so reducing power consumption. In this state the `MASTERCLK` signal becomes a 100R pull up to +5v. When this bit is set, `MASTERCLK=4MHz`. Remember to set this bit as part of your initialisation if you require the on-card clock.

## ***BANKn DIR CTRL REGISTERS (IDX 8,9,A,B,C)***

These five registers control whether each bank is set for input/output/open drain operation. BANK0 differs from the other 4 banks. The register layout is as follows:

### **BANK0 DIR CTRL**

BIT0	IOPIN 1 DIRECTION
BIT1	IOPIN 2 DIRECTION
BIT2	IOPINS 3&4 DIRECTION
BIT3	IOPINS 5,6,7&8 DIRECTION
BIT4	SET BANK OUTPUTS TO OPEN DRAIN OPERATION
BIT5..7	NOT USED

### **BANK1,2,3&4 DIR CTRL**

BIT0	BANK DIRECTION
BIT1	NOT USED
BIT2	NOT USED
BIT3	NOT USED
BIT4	SET BANK OUTPUTS TO OPEN DRAIN OPERATION
BIT5..7	NOT USED

In all cases, a logic '1' sets the IOPIN(s) or BANK to an output. A logic '1' in BIT 4 enables the open drain function. In this mode, each IOPIN is pulled via a 47K resistor to Vpull as set via the AUX SETUP REGISTER. The IOPIN rise time in this mode is load dependant. The IOPIN will typically reach between 4.6v and 4.8v when pulled high although the exact level will depend on the host-controllers VCC level. By programming an IOPIN as an input, Vpull and the IOPIN's 47K resistor could be used for diagnostics e.g. trying to pull a signal line around to test that it is not being driven.

## ***TIMER 0,1&2 REGISTERS (IDX 10h,11h,12h)***

These registers access the UPD71054's (NEC) counter timers. These registers are used for reading and writing count values. Refer to any 8254 compatible data sheet for full programming details (e.g. NEC, INTEL etc.).

## ***TIMER CTRL REGISTER (IDX 13h)***

This register is used for setting the counter/timer modes (CTmodes) for the three counter timers as described above.

## 3.0 HARDWARE SPECIFICATION

### DIGITAL I/O:

- Programmable as Input/Output allowing any number of inputs and outputs from 0 to 40.
- An I/O set as an output can be read-back for verification purposes. An I/O set as an output can also be set into open drain mode. Input levels are TTL compatible.
- Output drivers are CMOS, with typically 4mA source/sink at TTL levels.
- All I/Os have a 47K pull up/down resistor and will all power up as inputs. The pull direction is programmable to 0v or 5v (globally), defaulting to 0v on power-up.
- Readback can be "asynchronous" or latched. Asynchronous mode relies on software polling, whereas latched mode uses Timer 0 to strobe the input data into internal holding latches and the same strobe can generate an interrupt or be polled (if required). This applies globally to all I/Os set as inputs.
- All reads/writes to the card are 8-bits wide. All data and configuration registers can be read as well as written to make "bit-wise" updates easy.

### TIMERS

- 3-Channel counter/timer chip on card can be driven by user.
- Additionally, Timer 0 can be driven from a card generated 1MHz, 100KHz or 10KHz clock. This clock is also available to the user (duty cycles 50%,90%,90% respectively).
- Timer 0's gate is pulled high but can be over-driven by the user if required. It can also be driven from an internal control bit if required.
- The status of Timer 0's output can be read back for polling purposes.
- The programmable clock output can be tri-stated (47K pull-up) and over-driven by the user if required.
- The timer chip is an NEC 71054 (Intel 8254 compatible) and its control/data registers can be read/written by the software.
- Card's master 4MHz (+/-0.5% initial accuracy, 50% nominal duty cycle) clock output is available to user and can be turned off by software.
- There is also a single user interrupt input source that can be configured (rather than using Timer 0's output).

## MISCELLANEOUS

- PCMCIA interface uses 2-I/O ports to communicate with the card (Index & Data registers). These can be located on any even system I/O address. All transactions are 8-bits wide.
- Card has a fully PCMCIA compliant Card Information Structure and offers 2 configuration modes, WITH interrupts and WITHOUT interrupts. Card supports both Pulse and Level mode interrupts.
- Type II card uses a pair of highly durable 30-way flexible circuits and a connector PCB to interface all user signals. Two options are available: 60 way trigger terminal interface or 60 way half pitch IDC interface. Both options are interchangeable.
- Power consumption is typically 15mA at 5V with no loads attached, dropping to around 3mA in "SLEEP" mode (these figures are for guidance only and will depend on exact operational setup).
- "Hot-insertion" will not generate any spurious outputs on the 40 digital I/O lines.
- Frequency meter mode allows direct measurement of TTL signal frequencies from 1Hz to 8MHz using a single "loop-back" connection at the interface. Auto-ranging software allows accuracies of typically 0.5% from 40Hz to 8MHz to be realised.

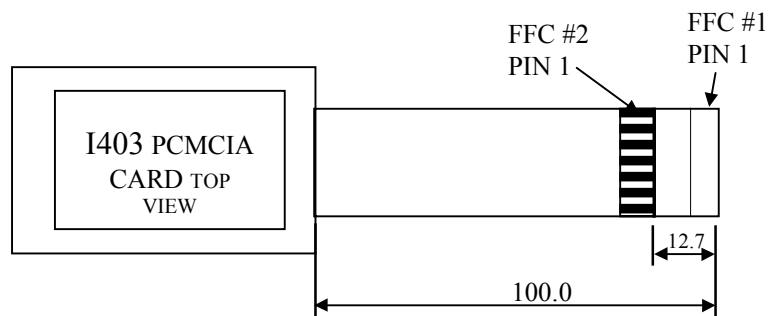
## PINOUTS

Signals are carried off the I403 using two 30 way Flat Flexible Conductors (FFC's). These are 1mm pitch types with ends prepared to fit into HIROSE FH10A-30S-1SHB type SMT connectors. The pitch between these should be 12.7mm with one mounted on the top surface and one of the rear surface of the connecting PCB. Care should be taken that the pin numbers on these connectors is made to match the pin numbering on the FFCs as shown below.

FFC#2 PIN NUMBER	SIGNAL	FFC#1 PIN NUMBER	SIGNAL
1	GND	1	GND
2	IOPIN2	2	IOPIN1
3	IOPIN4	3	IOPIN3
4	IOPIN6	4	IOPIN5
5	IOPIN8	5	IOPIN7
6	IOPIN10	6	IOPIN9
7	IOPIN12	7	IOPIN11
8	IOPIN14	8	IOPIN13
9	IOPIN16	9	IOPIN15
10	IOPIN18	10	IOPIN17
11	IOPIN20	11	IOPIN19
12	IOPIN22	12	IOPIN21
13	IOPIN24	13	IOPIN23
14	CTOUT0	14	CTGATE0
15	CTCLK1	15	CTCLK2
16	CTGATE1	16	CTGATE2
17	CTOUT1	17	CTOUT2
18	nUIRQ	18	VCC (200mA MAX)
19	N/C	19	GND
20	GND	20	CLKOUT
21	GND	21	MASTERCLK
22	GND	22	GND
23	IOPIN25	23	IOPIN26
24	IOPIN27	24	IOPIN28
25	IOPIN29	25	IOPIN30
26	IOPIN31	26	IOPIN32
27	IOPIN33	27	IOPIN34
28	IOPIN35	28	IOPIN36
29	IOPIN37	29	IOPIN38
30	IOPIN39	30	IOPIN40

### I403 PINOUTS

**NB: FFC#2 CONDUCTORS FACE UP, FFC#1 CONDUCTORS FACE DOWN**



### IDC BREAKOUT BOARD OPTION:

60 WAY HALF PITCH CONNECTOR TYPE: HIROSE HIF6H-60PA-1.27DS (PLUG) MATES WITH HIROSE HIF6H-60D-1.27R (CABLE MOUNTED SOCKET).

PINOUT:

PIN NUMBER	SIGNAL
1	GND
2	GND
3	IOPIN2
4	IOPIN1
5	IOPIN4
6	IOPIN3
7	IOPIN6
8	IOPIN5
9	IOPIN8
10	IOPIN7
11	IOPIN10
12	IOPIN9
13	IOPIN12
14	IOPIN11
15	IOPIN14
16	IOPIN13
17	IOPIN16
18	IOPIN15
19	IOPIN18
20	IOPIN17
21	IOPIN20
22	IOPIN19
23	IOPIN22
24	IOPIN21
25	IOPIN24
26	IOPIN23
27	CTOUT0
28	CTGATE0
29	CTCLK1
30	CTCLK2
31	CTGATE1
32	CTGATE2
33	CTOUT1
34	CTOUT2
35	nUIRQ
36	Vcc (200mA MAX)
37	N/C
38	GND
39	GND
40	CLKOUT
41	GND
42	MASTERCLK
43	GND
44	GND
45	IOPIN25
46	IOPIN26
47	IOPIN27
48	IOPIN28
49	IOPIN29
50	IOPIN30
51	IOPIN31
52	IOPIN32
53	IOPIN33
54	IOPIN34
55	IOPIN35
56	IOPIN36
57	IOPIN37
58	IOPIN38
59	IOPIN39
60	IOPIN40

## **4. SOFTWARE**

### ***4.1 UNIVERSAL DRIVER***

The PCCARDGO “universal driver” is used to act as a surrogate Card Services client for an end user application. This device driver simplifies greatly the enumeration process and configuration management task for your application.

The driver is supplied on the diskette provided.

Please refer to PCCARDGO.DOC for further information.

### ***4.2 C SOURCE CODE***

On the diskette provided are several .C and .H files that provide a convenient starting point for you to create your own application. The files are located in a directory with the same name as this card.

## 5.0 OPERATIONAL PRECAUTIONS

Unless otherwise stated, all voltage levels are referenced to the **I403**'s "GND" pins.

- DON'T LEAVE ACTIVE SIGNALS CONNECTED TO THE DIGITAL IOPINs OR OTHER DIGITAL LINES THAT ARE CAPABLE OF SOURCING MORE THAN A FEW mA WHILST THE I403 ITSELF IS UNPOWERED. THIS COULD LEAD TO "REVERSE POWERING" THE CARD VIA ITS INPUTS WHICH CAN CAUSE LATCH-UP AND DESTRUCTION OF INTERNAL CMOS DEVICES. IF THERE IS A POSSIBILITY OF THIS CONDITION OCCURRING, YOU ARE ADVISED TO CONNECT SERIES RESISTORS BETWEEN YOUR DRIVERS AND THE I403'S SIGNALS TO AFFECT CURRENT LIMITING (TYP 4K7). REMEMBER THAT THIS WILL SLOW THE EDGES OF THE DIGITAL SIGNALS.
- DON'T DRAW EXCESSIVE CURRENT FROM VCC. THE LIMITS ARE SHOWN IN THE PINOUT TABLE. DOING SO WILL ADVERSELY EFFECT THE I403'S PERFORMANCE AND COULD CAUSE DAMAGE.
- DON'T APPLY DIGITAL INPUTS TO THE I403 THAT ARE GREATER THAN (System Vcc + 0.5v) WHERE "System Vcc" IS THE LEVEL PROVIDED ON THE I403'S VCC OUTPUT PIN. DOING SO WILL DAMAGE THE I403. LIKEWISE, DON'T APPLY LEVELS THAT ARE LESS THAN -0.5v TO THE DIGITAL INPUTS.
- DON'T SHORT CIRCUIT ANY OF THE I403'S OUTPUTS TO GROUND OR TO OTHER OUTPUTS. THIS WILL DAMAGE THE I403.